CLAIMS

WHAT IS CLAIMED:

1. A semiconductor device, comprising:

a substrate including a contact pad;

a solder bump formed on said contact pad; and

an absorption layer disposed between said contact pad and said solder bump, said absorption layer having a thickness that is configured to substantially stop alpha particles of at least 5.4 MeV.

2. The semiconductor device of claim 1, wherein said absorption layer comprises at least one of copper, nickel, chromium, tungsten, gold, silver, platinum, tantalum and a compound thereof.

3. The semiconductor device of claim 1, wherein said absorption layer comprises two or more sub-layers.

4. The semiconductor device of claim 1, wherein said absorption layer is adapted to reduce passage of alpha particles to a rate less than 0.001 alpha particles/cm^2 an hour.

5. The semiconductor device of claim 1, wherein said absorption layer laterally extends beyond said solder bump.

6. The semiconductor device of claim 4, further comprising a passivation layer covering a peripheral portion of said absorption layer.

7. The semiconductor device of claim 1, further comprising a second solder bump formed over a second absorption layer, wherein said absorption layer and said second absorption layer are laterally isolated from each other by a spacing of approximately 1-100 μm.

8. The semiconductor device of claim 8, wherein said spacing is filled with a dielectric material.

9. The semiconductor device of claim 1, wherein a thickness of said absorption layer is in the range of approximately 1-10 μm.

10. The semiconductor device of claim 1, wherein an intrinsic alpha particle emission rate of said absorption layer is less than 0.001 alpha particles/cm^2 an hour.

11. A semiconductor device, comprising:

a substrate including a contact pad;

a solder bump formed on said contact pad; and

an underbump metallization disposed between said contact pad and said solder bump, said underbump metallization substantially preventing diffusion of solder bump material into said substrate and providing adhesion of said solder bump to said substrate, wherein said underbump metallization has a thickness sufficient to stop alpha particles of approximately 5.4 MeV.

12. The semiconductor device of claim 11, wherein an intrinsic alpha particle emission rate of said underbump metallization is less than 0.001 alpha particles/cm^2 an hour

13. The semiconductor device of claim 11, wherein a thickness of said underbump metallization is in the range of approximately 1-10 μm.

14. The semiconductor device of claim 11, wherein said underbump metallization comprises an absorption layer having a thickness of approximately 1 μm or more.

15. The semiconductor device of claim 14, wherein said absorption layer comprises at least one of copper, nickel, tungsten, gold, silver, platinum, tantalum and any compound thereof.

16. The semiconductor device of claim 11, wherein a lateral extension of said underbump metallization is larger than a lateral extension of said solder bump.

17. The semiconductor device of claim 14, wherein a thickness of said absorption layer is in the range of approximately 1-10 μm.

18. The semiconductor device of claim 11, wherein a peripheral portion of said underbump metallization is coated with a passivation layer.

19. A semiconductor device, comprising:

a substrate including a functional element;

a multilayer metal stack formed over said substrate, wherein said multilayer metal stack has an intrinsic alpha particle emission rate of less than 0.001 alpha particles/cm^2 an hour and a thickness of 1 μm and more; and

a solder bump formed on said multilayer metal stack.

20. The semiconductor device of claim 19, wherein said multilayer metal stack laterally extends beyond said solder bump.

21. The semiconductor device of claim 19, further comprising a passivation layer covering a peripheral portion of said multilayer metal stack.

22. The semiconductor device of claim 19, wherein said multiplayer metal stack comprises at least one of copper, nickel, tungsten, gold, silver, platinum, tantalum and any compound thereof.

23. A method of forming a soft error reduced semiconductor device, the method comprising:

providing a substrate having formed thereon a circuit element;

forming a contact pad over said substrate;

forming an electrically conductive absorption layer over said contact pad with a predefined thickness allowing the stoppage of alpha particles with an energy of approximately 5.4 MeV; and

forming a solder bump over said absorption layer.

24. The method of claim 23, wherein forming said absorption layer comprises depositing said absorption layer and controlling at least one process parameter to obtain said predefined thickness.

25. The method of claim 23, further comprising forming at least one further metal layer adjacent to said absorption layer.

26. The method of claim 25, wherein a total thickness of said further metal layer and said absorption layer is in the range of approximately 1-10 μm.

27. The method of claim 23, wherein said predefined thickness of said absorption layer is in the range of approximately 1-10 μm.

28. The method of claim 23, further comprising forming a second solder bump over said absorption layer, and forming a trench between said solder bump and said second solder bump to electrically insulate said solder bump and said second solder bump.

29. The method of claim 28, wherein a width of said trench is in the range of approximately 1-100 μm.